Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **IN –**
2. **IN +**
3. **VCC –**
4. **OUT**
5. **VCC +**

**.035”**

**.048”**

**1**

**2**

**3**

**5**

**4**

**MASK**

**REF**

**THS**

**3001**

**E**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref: THS3001 E**

**APPROVED BY: DK DIE SIZE .035” X .048” DATE: 11/10/20**

**MFG: NSC / Texas Instruments THICKNESS .011” P/N: THS3001**

**DG 10.1.2**

#### Rev B, 7/1